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Declaration



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On July 25, 2003

TOWNSEND and TOWNSEND and CREW LLP

By: Thane Currier Cass

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Hong Koo Kim

Application No.: 09/747,779

Filed: December 22, 2000

For: FABRICATION METHOD AND
STRUCTURE FOR FERROELECTRIC
NONVOLATILE MEMORY FIELD
EFFECT TRANSISTOR

Examiner: Marcos D. Pizarro Crespo

Art Unit: 2814

DECLARATION OF HONG KOO KIM
UNDER 37 C.F.R. § 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Professor HONG KOO KIM, declare:

1. I am a U.S. citizen, residing at 1611 Country Club Drive, Pittsburgh, PA 15237, and am a professor in Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania, and have been a faculty member of the University of Pittsburgh since 1990 (assistant professor from 1990 to 1996, associate professor from 1996 to 2002, and full professor since 2002).

2. I attended Seoul National University in Korea from 1977 to 1981 and received a Bachelor of Science degree in Electronics Engineering, and Korea Advanced Institute of Science and Technology from 1981 to 1983 and a Master of

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Science degree in Electrical Engineering, and Carnegie Mellon University in Pennsylvania from 1986 to 1989 and a Philosophy of Doctor degree in Electrical and Computer Engineering.

3. Since 2002, I have been Co-Director of the Institute of NanoScience and Engineering at the University of Pittsburgh. Since 1996, I have been Chair of the Western Pennsylvania Chapter of the American Vacuum Society. I have been a member of IEEE, Materials Research Society, and American Physical Society.

4. From 1983 to 1986, I had been a research staff at the Electronics and Telecommunications Research Institute in Korea.

5. I published over 50 refereed papers in the area of microelectronics, optoelectronics and nanophotonics, including the following papers on the ferroelectric nonvolatile memory devices: 1) "Ferroelectric nonvolatile memory field-effect transistors based on a novel buffer layer structure", Hong Koo Kim and Nasir Abdul Basit, International Journal of High Speed Electronics and Systems, vol.10, 39-46, 2000 (Invited Paper), 2) "Growth of highly oriented Pb(Zr,Ti)O₃ films on MgO-buffered oxidized Si substrates and its application to ferroelectric nonvolatile memory field-effect transistors", Nasir Abdul Basit and Hong Koo Kim, Applied Physics Letters, vol.73, 3941-3943, 1998, and 3) "Lead-zirconate-titanate-based metal/ferroelectric/insulator/semiconductor structure for nonvolatile memories", Mingjiao Liu, Hong Koo Kim, and Jean Blachere, Journal of Applied Physics, vol.91, 5985-5996, 2002.

6. I am an inventor of the above-identified U.S. Patent Application No 09/747,779, filed on December 22, 2000, which claims priority to Provisional U.S. Patent Application No. 60/173,199, filed on December 27, 1999. This application relates to ferroelectric nonvolatile memory field effect transistors. I have read and understood this patent application and the claims now pending therein.

7. Embodiments of the present invention solved a major problem in developing a ferroelectric field-effect transistor (FEFET) structure for nonvolatile memory device applications. The well-known problem in this field has been on

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integrating a ferroelectric layer on a silicon FET structure without sacrificing/compromising the characteristics of each part, i.e., an FET and a ferroelectric layer. Direct deposition of a ferroelectric layer on silicon surface usually results in poor interface properties (due to reaction or interdiffusion between the two materials during film deposition or post-deposition annealing processes). This has detrimental effects on the FET channel and the ferroelectric layer. Deposition of ferroelectric material on amorphous surface (i.e., oxidized silicon surface) usually results in an amorphous phase of the material which is either nonferroelectric or very weakly ferroelectric. Any attempt to grow oriented films that show ferroelectric property usually results in intermixing between ferroelectric and oxidized silicon due to the high temperature process involved. In prior work, a buffer layer of certain insulating materials (such as CeO_2 , CaF_2 or SrTiO_3) has been introduced between silicon and ferroelectric in order to alleviate this problem. Being directly deposited on crystalline surface of silicon, these buffer layers are usually grown highly oriented and are used as a template to deposit an oriented ferroelectric layer. While this structure shows improved interface properties compared with the ferroelectric/silicon structure, it still suffers from the problems of poor retention, carrier injection, and large leakage current.

In one embodiment we overcome this problem by employing the following materials system, layer structure and process steps: 1) Grow first a thin layer of amorphous silicon oxide on silicon surface using a standard thermal oxidation process in dry oxygen ambient. This oxidation process, commonly used in standard CMOS processes, is well known to provide the best quality of silicon surface passivation and thus the best properties of FET channels. 2) Grow an oriented buffer layer (MgO) on top of the thermally grown amorphous silicon oxide. This inventor has discovered that MgO can be grown highly oriented on amorphous silicon-oxide surface under certain process conditions. 3) Grow an oriented ferroelectric layer (for example, PZT) on top of the MgO buffer using the buffer layer as a template. The MgO is also found to well serve as a diffusion barrier between PZT and oxidized silicon.

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8. I have read and understood the rejection in the final Office Action mailed on February 25, 2003. I have also read and understood the cited art in the final Office Action, including Hirai et al. (U.S. Patent No. 5,955,755), Kirin et al. (U.S. Patent No. 5,225,561), and Maiti et al. (U.S. Patent No. 6,020,024), that the Examiner has used to reject claims 1, 3-10, and 14-22. I have also reviewed the Amendment Under 37 C.F.R. § 1.116 mailed on April 25, 2003 and the Advisory Action mailed on May 20, 2003 by the Examiner in response to the Amendment Under C.F.R. § 1.116.

9. I have reviewed the Preliminary Amendment filed with the present Request for Continued Examination and the pending claims therein. The pending claims have been amended to clarify that

First, a silicon oxide layer is formed on silicon surface using a thermal oxidation process without any prior deposited material on the silicon surface. As well known by those skilled in the art, forming a silicon oxide layer directly on the silicon surface provides high-quality passivation of silicon surface, thereby providing enhanced FET channel characteristics.

Second, an oriented, insulating buffer layer (MgO) is formed on an amorphous silicon-oxide layer, rather than on silicon surface that has a crystalline structure. This process is based on our findings that a certain insulating material (such as MgO) can be grown self-oriented on amorphous surface (such as silicon oxide) under certain process conditions and thus can be used as a template to grow oriented ferroelectric layers (such as PZT).

Overall this embodiment is clearly different from that of Hirai et al. in which an oriented buffer layer is first formed on crystalline silicon surface and then a silicon oxide layer is formed sandwiched in between the silicon and insulating buffer by thermal annealing them in oxygen ambient. A silicon oxide resulting from the Hirai process is generally of lower quality than the silicon oxide formed directly on the silicon surface. The fact that Hirai discloses formation and use of the lower quality silicon oxide indicates to me that its inventors did not know how to form an oriented buffer layer on a

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non-crystalline surface. The claims now pending in this application are clearly patentable over Hirai, Kirin, and Maiti.

10. Although the overall layer structure of the FEFET device discussed in this embodiment (metal/ferroelectric/insulating-buffer/silicon-oxide/silicon) has certain similarity to that of Hirai, the processes used in forming a silicon oxide buffer is very different in the two processes. Accordingly, the properties of the resulting silicon/silicon-oxide interface are expected to be different. In Hirai's method, an insulating buffer layer is grown directly on a crystalline silicon surface in order to obtain an oriented buffer layer. A silicon oxide layer is then formed by annealing the buffer-layer-covering the silicon surface in oxygen ambient. As such, the nature of Hirai's silicon surface passivation cannot be the same as that of this embodiment, which employs a thermal oxidation on free silicon surface without any prior deposited material thereon.

11. Hirai, Kirin, and Maiti, alone or in combination, fail to disclose or suggest the claimed method of fabricating the non-volatile memory. Without providing any supporting information, Hirai et al. claimed that an alternative process sequence may be performed to implement the metal/ferroelectric/insulating-buffer/silicon-oxide/silicon structure, i.e., first form a silicon oxide layer and then an insulating buffer and a ferroelectric layer (U.S. Patent No. 5,955,755 column 7 line 66 to column 8 line 9). It is generally believed in this field that insulating materials usually do not grow self-oriented on amorphous surface. There is no suggestion in Hirai that they are aware of that MgO (or any other insulating buffer layer listed in their patent) has a tendency to grow self-oriented on amorphous surface. There is no disclosure in Hirai that they utilize this special property in their invention. Hirai describes six fabrication methods. All of them disclose forming an oriented buffer layer directly on crystalline silicon and then performing thermal annealing for silicon oxide formation. No explicit statement or supporting information is given about the possibility and utilization of forming a self-oriented buffer layer on amorphous surface.

12. The nature of the thermal annealing steps employed for the insulating buffer layers is also different for the two processes. In the present

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embodiment, the purpose of this annealing step is to enhance the crystalline property of the deposited layer, i.e., to make it a highly oriented buffer layer grown on an amorphous surface. The MgO buffer layer is found to grow highly oriented on silicon oxide surface under the deposition and post-deposition annealing conditions disclosed in this embodiment. In the Hirai et al., the deposited buffer layer is grown oriented due to the template role played by the crystalline silicon surface. The purpose of their annealing step is then to form a silicon oxide layer at the interface between the buffer layer and silicon. In this annealing process of Hirai, oxygen is expected to diffuse through the buffer layer and to reach the silicon interface.

13. Considering the different conditions of silicon surface passivation (The silicon surface in Hirai is already covered/interfaced with an insulating buffer material, whereas the silicon surface in this invention is crystalline, free from any deposited material.), the resulting silicon interface properties (surface/interface states, etc.) are expected to be different between the two cases. Thermal oxidation of free silicon surface is the preferred way of passivating silicon surface in the standard CMOS processes due to resulting good FET channel properties. The FEFET devices thus fabricated show excellent performances in ferroelectric polarization switching and memory retention. (Please see the attached papers: Growth of highly oriented $\text{Pb}(\text{Zr,Ti})\text{O}_3$ films on MgO-buffered oxidized Si substrates and its application to ferroelectric nonvolatile memory field-effect transistors," Applied Physics Letter, Vol. 73, No. 26; and "Lead-zirconate-titanate-based metal/ferroelectric/insulator/semiconductor structure for nonvolatile memories," Journal of Applied Physics, Vol. 91, No. 9.)

14. I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

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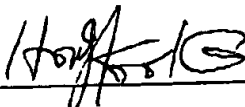
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Date: July 24, 2003


Hong Koo Kim

PA 3312450 v1

Lead-zirconate-titanate-based metal/ferroelectric/insulator/semiconductor structure for nonvolatile memory

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We have investigated the structural and electrical properties of the metal/ferroelectric/insulator/semiconductor (MFIS) structure that incorporates a MgO/SiO_2 insulating buffer between a ferroelectric layer and Si substrate. Highly oriented lead-zirconate-titanate [$\text{Pb}(\text{Zr,Ti})\text{O}_3$, or PZT] films were grown on the MgO-buffered oxidized silicon substrates with a rf magnetron sputtering technique. The x-ray diffraction and energy-dispersive x-ray spectroscopy analysis results show that a MgO buffer serves well not only as a template layer for growing oriented PZT films on an amorphous surface but also as a diffusion barrier between PZT and Si substrates. The memory window of the MFIS structure was characterized with a capacitance-versus-voltage method. Numerical analyses were also carried out to simulate the MFIS capacitor characteristics. In this simulation, the PZT films were assumed to have a two-layer structure in which the dielectric and ferroelectric properties of an initial layer are significantly weaker than those of the main layer part. By comparing the measurement data with the simulation result, we have extracted the parameters of this two-layer model (dielectric constant and the polarization-versus-electric-field characteristics) of the PZT films in the MFIS structure. The scalability of the memory window of the MFIS structure was investigated by varying the ferroelectric (PZT) layer thickness. Both the experimental and simulation results show that the PZT-based MFIS structure is suitable for nonvolatile memory field-effect transistors with low-voltage requirement (3 V or less) and large memory window (1–2 V). © 2002 American Institute of Physics. [DOI: 10.1063/1.1465504]

I. INTRODUCTION

Nonvolatile memory devices retain information even in the absence of applied power.¹ Demand for such devices has been growing as many electronic products become more portable and wireless. Nonvolatile memory technologies are expanding in response to this increasing need, and are further advancing towards the ultimate goal of memory: low-voltage, low-power, and high-speed operation for reading and writing, infinite retention time, infinitely rewritable, scalable in physical dimension, radiation hard, and inexpensive.² The ferroelectric field-effect transistors (FEFETs) are promising as a nonvolatile memory device that offers most of the ideal characteristics listed above. A FEFET consists of a FET whose gate dielectric is comprised of a ferroelectric material or a stack of dielectrics with a ferroelectric layer.^{3–5} The application of a voltage pulse to the gate sets the direction of the ferroelectric polarization. The polarization direction controls the electrical conductance of the channel under the ferroelectric, and thus the drain current of the FET. The binary level of the channel conductance can be used to define two logic states, and can be read without destroying the ferroelectric polarization.

Despite the unique advantages offered by the device structure, realization of commercially viable FEFETs has been hampered by some technical difficulties. Basically, the

challenge is in integrating a ferroelectric gate structure on the surface of the FET channel region, which usually results in poor interface properties and, therefore, in poor memory retention.^{6,7} Recently, we have reported FEFET memory devices that incorporate a metal/ferroelectric [$\text{Pb}(\text{Zr,Ti})\text{O}_3$]/insulator (MgO/SiO_2)/semiconductor (MFIS) structure as a gate of a silicon FET.⁸ A MgO buffer was introduced as a template layer for growth of oriented PZT films and also as a diffusion barrier between PZT and Si, while thermally grown SiO_2 was used for passivation of the Si surface. FEFET devices thus fabricated show excellent performance in ferroelectric polarization switching and memory retention, suggesting good interface properties between ferroelectric and Si.

The switching performance (memory window and operating voltage) of a FEFET is basically determined by the structural and materials properties of the MFIS structure (i.e., the thickness and ferroelectric/dielectric properties of each layer).⁴ It is of great importance to establish a relationship between the layer thickness and the switching performance in the PZT/MgO/SiO₂/Si structure for optimum design of the FEFET devices. In this work, we have investigated the scalability of switching performance (i.e., the feasibility of low-voltage operation with a large memory window) of the MFIS structure by varying the ferroelectric (PZT) layer thickness. Numerical analyses were also carried out to simulate the capacitor characteristics of the MFIS structure. The PZT films

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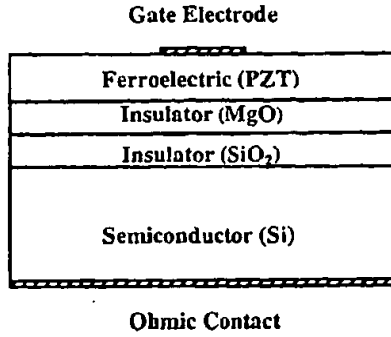


FIG. 1. Schematic drawing of a metal-ferroelectric-insulator-semiconductor (MFIS) capacitor structure.

were assumed to have a two-layer structure in which the dielectric and ferroelectric properties of an initial bottom layer are significantly weaker than those of the top layer part. By comparing the simulation result with the experimental data, we have also extracted the key parameters of the polarization switching characteristics (i.e., the remnant and saturated polarizations and the coercive electric field) of the PZT films grown on MgO-buffered substrates.

II. MFIS CAPACITOR THEORY

Figure 1 shows a schematic drawing of the metal-ferroelectric-insulator-semiconductor capacitor structure that we have investigated in this study. In this section, we provide a brief review of the MFIS capacitor theory in order to help understand the experimental and simulation results presented in this article. The ferroelectric polarization can control the status of a semiconductor surface region, i.e., it can enhance accumulation of majority carriers, or form an inversion layer (channel) by inducing minority carriers. Let us consider the case in which the gate bias voltage is swept from the negative to the positive direction. First, a proper amount of negative gate voltage would make the ferroelectric polarization direct towards the gate. As the gate voltage is increased towards the positive direction, some of the ferroelectric polarization will switch the direction, pointing towards the substrate side. The majority of the polarization, however, remains unchanged until the applied electric field reaches a certain point, which is called the coercive field of the ferroelectric. For gate voltages greater than this critical point, the majority of the ferroelectric polarization will switch the direction. Now, consider a return sweep, i.e., a gate voltage is swept from the positive to the negative direction. Similar to the previous case, the polarization will remain unchanged until the gate voltage reaches a proper negative value that corresponds to the negative coercive field of the ferroelectric. Overall, this would result in a clockwise hysteresis in C - V curves.

The voltage applied across a MFIS capacitor can be expressed as the sum of the voltage drops that appear across each layer and in the Si region:

$$V_g = E_f t_f + E_{\text{MgO}} t_{\text{MgO}} + E_{\text{SiO}_2} t_{\text{SiO}_2} + \phi_s, \quad (1)$$

where E_f , E_{MgO} , and E_{SiO_2} are the electric field in the ferroelectric, MgO, and SiO_2 layers, respectively, and likewise, t_f , t_{MgO} , and t_{SiO_2} are the thickness of the corresponding layers. ϕ_s is the potential at the Si surface. Assuming no trapped charges exist at each layer interface, and applying the Gauss theorem on the layer interfaces, we can obtain the following relationship among the electric fields in each layer:

$$\epsilon_f E_f + P_d = \epsilon_{\text{MgO}} E_{\text{MgO}} = \epsilon_{\text{SiO}_2} E_{\text{SiO}_2} = -\sigma_s, \quad (2)$$

where ϵ_f is the linear dielectric constant of the ferroelectric layer, which does not include the effect of ferroelectric polarization switching. P_d is the switchable polarization in the ferroelectric layer. ϵ_{MgO} and ϵ_{SiO_2} are the dielectric constants of the MgO and SiO_2 buffer layers, respectively. σ_s is the total amount of charge in the silicon region, which can be expressed as a function of the Si surface potential ϕ_s , as follows:⁹

$$\sigma_s(\phi_s) = -\text{SGN}(\phi_s) \sqrt{2} \frac{kT \epsilon_0 \epsilon_s}{q} \frac{1}{L_B} \left(\left(e^{-q\phi_s/kT} + \frac{q}{kT} \phi_s - 1 \right) + \left(\frac{n_i}{N_a} \right)^2 \left(e^{q\phi_s/kT} - \frac{q}{kT} \phi_s - 1 \right) \right)^{1/2}, \quad (3)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, and bulk Debye length L_B is given by

$$L_B = \left(\frac{kT \epsilon_0 \epsilon_s}{q^2 N_a} \right)^{1/2}. \quad (4)$$

The gate voltage at the threshold point can then be expressed as follows:

$$V_t = -\frac{P_d}{C_f} - \frac{\sigma_s}{C_{\text{stack}}} + \phi_{s(\text{inv})}, \quad (5)$$

where $\phi_{s(\text{inv})}$ is the surface potential of Si at the threshold point. [Here, the threshold point is defined as the onset of strong inversion in the Si surface region, the same as in the regular metal-oxide-semiconductor (MOS) capacitor case.⁹] C_f represents the capacitance component of the ferroelectric layer that excludes the contribution from the switchable polarizations, and is given by

$$C_f = \frac{\epsilon_f}{t_f}. \quad (6)$$

C_{stack} is the stacked capacitance of the ferroelectric and dielectric buffer layers, and is given by

$$C_{\text{stack}} = \left(\frac{t_f}{\epsilon_f} + \frac{t_{\text{MgO}}}{\epsilon_{\text{MgO}}} + \frac{t_{\text{SiO}_2}}{\epsilon_{\text{SiO}_2}} \right)^{-1}. \quad (7)$$

P_d is a function of the electric field in the ferroelectric layer as well as the field history. As the dc bias is swept back and forth between positive and negative voltages, the switchable ferroelectric polarization shows a hysteresis behavior. This would result in a threshold voltage shift, and the amount of the voltage shift is given by

$$\Delta V_{th} = -\frac{\Delta P_d}{C_f} \quad (8)$$

The amount of ferroelectric polarization switching ΔP_d is mainly determined by the peak electric field applied across the ferroelectric layer during the positive- and negative-going voltage sweeps.

The saturated polarization hysteresis loop is usually described with the following analytic function.^{10,11} (Here, it should be mentioned that this does not have a physical derivation but comes from curve fitting and mathematical convenience.)

$$P_{ds}^+(E) = P_s \tanh\left[\frac{E - E_c}{2\delta}\right], \quad (9)$$

where

$$\delta = E_c \left[\log \frac{1 + \frac{P_r}{P_s}}{1 - \frac{P_r}{P_s}} \right]^{-1} \quad (10)$$

P_s is the saturated polarization, which would result when all the dipoles are fully aligned. P_r is the remnant polarization at zero electric field across a ferroelectric layer. E_c is the coercive field at which the polarization is zero. The hysteresis has two branches, $P_{ds}^+(E)$ for the positive-going electric field, $P_{ds}^-(E)$ for the negative-going field. When the hysteresis is symmetric, the two branches are related to each other as follows:

$$P_{ds}^-(E) = -P_{ds}^+(-E). \quad (11)$$

The P - E curves show an unsaturated behavior when the peak electric field is not large enough to make all the dipoles fully align along the electric field. The derivative of the unsaturated polarization curve $P_d(E)$ is related to the saturated hysteresis loop as follows:

$$\frac{\partial P_d}{\partial E} = \Gamma \frac{\partial P_{ds}}{\partial E}, \quad (12)$$

where

$$\Gamma = 1 - \tanh\left[\left(\frac{P_d - P_{ds}}{\xi P_s - P_d}\right)^{1/2}\right], \quad (13)$$

$\xi = 1$ for increasing electric field and $\xi = -1$ for decreasing electric field. Hysteresis curves $P_d(E)$ can then be obtained by integrating Eq. (12).^{4,11}

The following sequence of analyses was then carried out to investigate the dependence of the memory window on MFIS capacitors structural and materials parameters (i.e., the layer thickness and dielectric/ferroelectric properties) as well as the operating condition (i.e., the sweep voltage). First, from Eqs. (1), (2), and (3), the electric field in the ferroelectric layer is calculated as a function of the capacitor voltage applied in a given voltage sweep. The polarization hysteresis loops (P - E and P - V) are then calculated using Eq. (9) [or with the integration result of Eq. (12)]. The amount of ferro-

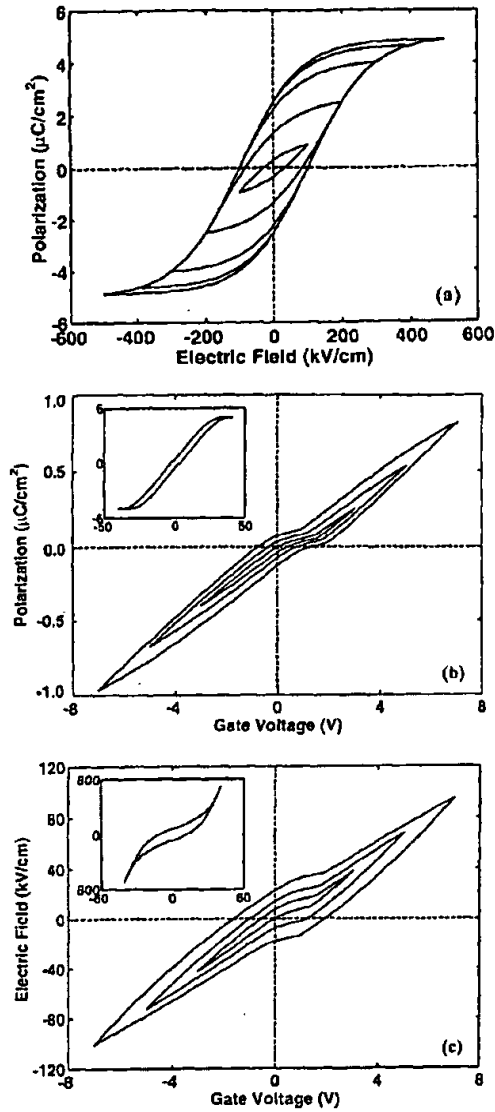


FIG. 2. Simulation example of the ferroelectric hystereses that were calculated with the following model parameters for a PZT film: $P_s = 5 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.5$, and $E_c = 100 \text{ kV}/\text{cm}$: (a) Ferroelectric polarization P_d vs electric field E_f . The peak electric field was varied from ± 100 to $\pm 500 \text{ kV}/\text{cm}$ with a $100 \text{ kV}/\text{cm}$ step. (b) Ferroelectric polarization vs gate voltage V_g in a metal/PZT($0.2 \mu\text{m}$)/MgO(10 nm)/SiO₂(10 nm)/Si structure. The gate voltage was swept for ± 3 , ± 5 , and $\pm 7 \text{ V}$. The inset shows a saturated hysteresis curve obtained with $\pm 40 \text{ V}$ sweep. (c) The electric field in the PZT layer vs the gate voltage in the same MFIS structure as analyzed in (b). The inset shows the case with $\pm 40 \text{ V}$ sweep.

electric polarization switching is then read from the P - V hysteresis curves, and the memory window is calculated using Eq. (8).

Figure 2(a) shows an example of the simulated P - E curves that were calculated with the following model parameters assumed for a ferroelectric layer: $P_s = 5 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.5$, and $E_c = 100 \text{ kV}/\text{cm}$. The peak electric field in PZT was varied from ± 100 to $\pm 500 \text{ kV}/\text{cm}$ with a 100

kV/cm step. In the case of a metal/ferroelectric (PZT)/metal (MFM) capacitor structure with a 0.2- μm -thick PZT, this peak electric field would correspond to a capacitor voltage of ± 2 to ± 10 V. It should be noted that the P - E curves do not show clear saturation until the peak electric field is increased over ± 300 kV/cm, which is approximately three times the coercive field value assumed in this P - E model. Figures 2(b) and 2(c) show the polarization versus gate voltage (P - V) and the electric field in PZT versus gate voltage (E - V) curves, respectively, that are calculated with the following structural and materials parameters assumed for the MFIS structure: PZT (0.2 μm thick, $\epsilon_f = 20\epsilon_0$, $P_s = 5 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.5$, and $E_c = 100$ kV/cm), MgO (10 nm thick with $\epsilon_{\text{MgO}} = 8.9\epsilon_0$), and SiO_2 (10 nm thick with $\epsilon_{\text{SiO}_2} = 3.9\epsilon_0$). The substrate is assumed to be p -type doped with $N_a = 3 \times 10^{16} \text{ cm}^{-3}$. The capacitor voltage (i.e., gate voltage V_g) was swept for ± 3 , ± 5 , and ± 7 V. The P - V curves do not show any clear saturation in this voltage range. The inset shows the case of saturation, which would require over 40 V gate voltage. This near-linear behavior of polarization in the relatively low-voltage sweeps can be understood in view of Fig. 2(c), which shows the peak electric field in PZT is smaller than the coercive field of saturated P - E curves. The peak electric field, for example, is read to be $+39/-42$ kV/cm for ± 3 V sweep, $+68/-73$ kV/cm for ± 5 V, and $+96/-101$ kV/cm for ± 7 V. [The inset in Fig. 2(c) shows the case with ± 40 V sweep.] These values are significantly smaller than those that can be obtained in a metal/PZT/metal capacitor structure for the same amount of voltage sweeps [Fig. 2(a)]. The reduction of the electric field in a MFIS structure is ascribed to the voltage drop that appears across the MgO/ SiO_2 buffer layers and in the silicon surface region. In the case of ± 7 V gate voltage applied on the MFIS structure described above, for example, the voltage drops across the MgO and SiO_2 buffer layers and in the Si region are calculated to be 1.5, 3.3, and 0.2 V, respectively, and the PZT layer gets 2.0 V. (The electric fields in the MgO and SiO_2 buffer layers are calculated to be 1.5 and 3.3 MV/cm, respectively, at the gate voltage of $+7$ V.) It is also interesting to note that the amount of polarization switching ΔP_d in the MFIS structure is significantly smaller than that in a MFM capacitor of the same PZT thickness with the same peak electric field. For example, ΔP_d is read to be $0.2 \mu\text{C}/\text{cm}^2$ in the P - V curve with ± 7 V voltage sweep (i.e., with the peak electric field of $+96/-104$ kV/cm), whereas the P - E curve in Fig. 2(a) shows ΔP_d of $0.6 \mu\text{C}/\text{cm}^2$ for the same strength of peak electric field (i.e., ± 100 kV/cm). The reduction of polarization switching in the MFIS capacitor structures is known to be an intrinsic phenomenon, and is explained by the fact that the ferroelectric field in a MFIS structure reverses the direction when the gate voltage is reduced from a peak value back to 0 V, as can be seen in Fig. 2(c).⁴ The physical origin of this behavior can be understood in reviewing the nature of the boundary conditions set at the ferroelectric/dielectric/semiconductor interfaces. The boundary condition in Eq. (2) shows coupling among the ferroelectric polarization (P_d), the electric field in a ferroelectric layer (E_f), and the gate voltage (V_g) via the surface charges in Si (σ_s). In the case of a MFM capacitor structure, there is no

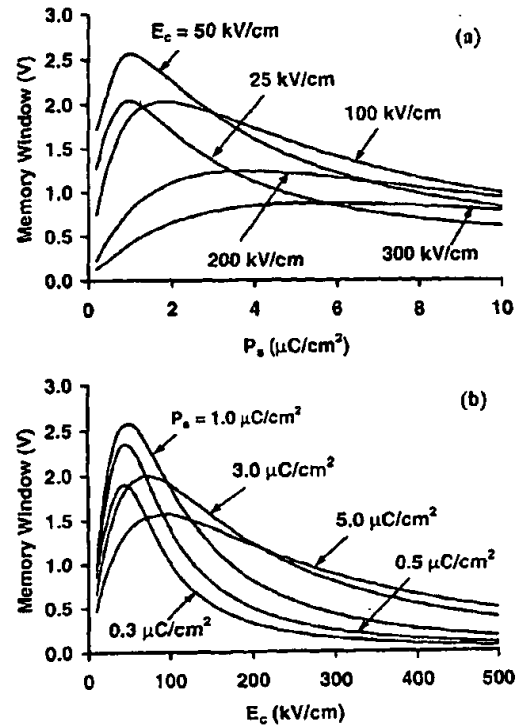


FIG. 3. (a) Memory window vs saturated polarization for various different coercive field of 25, 50, 100, 200, and 300 kV/cm. (b) Memory window vs coercive field for various saturated polarization values of 0.3, 0.5, 1.0, 3.0, and 5.0 $\mu\text{C}/\text{cm}^2$. The layer structure is assumed to be the same as that for Figs. 2(b) and 2(c), and the voltage sweep was ± 5 V.

such coupling, and therefore, the ferroelectric polarization is directly determined by the electric field (and the field history). In the case of the MFIS capacitors, however, any change in the Si surface charges, i.e., a transition from the depletion to the inversion or to the accumulation regimes, affects the electric field in each layer and, therefore, the ferroelectric polarization. This results in a kink and slight asymmetry in the P - V hysteresis.⁴ From the P - V curves shown in Fig. 2(b), the amount of polarization switching is read to be 0.04, 0.10, and $0.20 \mu\text{C}/\text{cm}^2$ for the sweep voltages of ± 3 , ± 5 , and ± 7 V, respectively. Using Eqs. (8) and (6) with $\epsilon_f = 20\epsilon_0$, the memory window is calculated to be 0.5, 1.1, and 2.3 V, respectively.

We have also calculated the dependence of the memory window of the MFIS structure on the ferroelectric properties (primarily the saturated polarization P_s and the coercive field E_c). Figure 3(a) shows the memory window versus saturated polarization for various different coercive fields of 25, 50, 100, 200, and 300 kV/cm. The layer structure is assumed to be the same as that for Figs. 2(b) and 2(c), and the voltage sweep was ± 5 V. For a given coercive field, each profile reveals two regimes, i.e., the memory window shows an initial sharp increase for relatively low-polarization values, and then it gradually falls off for larger polarization. These opposite trends can be explained as follows. Increasing the saturated polarization has the effect of increasing the rem-

nant polarization and also reducing the peak electric field in PZT. The former has the effect of increasing the memory window, since the P - E curve is stretched out along the P -axis direction. The latter has the opposite effect (i.e., reducing the memory window), since increasing the saturated polarization would result in an increase of the effective dielectric constant of the PZT layer (as will be discussed in Sec. IV), and thus a decrease of the voltage drop across the PZT. This would reduce the peak electric field and, therefore, the memory window. The former effect is found to be dominant in the low-polarization regime, and the latter one in the large-polarization regime. In between the two regimes, there is a peak that corresponds to a maximum memory window. A similar behavior is observed in the dependence of the memory window on the coercive field with the saturated polarization as a parameter [see Fig. 3(b)]. At $P_s = 1 \mu\text{C}/\text{cm}^2$, for example, the memory window initially shows an increasing trend for E_c of 25–50 kV/cm and then a monotonic decrease for E_c of greater than 50 kV/cm.

III. EXPERIMENT

The PZT-based MFIS structure was fabricated on Si substrates using rf magnetron sputtering of a stoichiometric $\text{Pb}(\text{Zr,Ti})\text{O}_3$ target (Zr:Ti ratio of 53:47). Previously, we have reported on crystallization of PZT films sputter deposited on Pt-buffered oxidized silicon substrates using a stoichiometric PZT target.¹² PZT films deposited at 200 °C or below were found to crystallize into a perovskite phase upon receiving an anneal treatment at 590 °C or above for 5–20 min. In this work, we have applied the low-thermal-budget process (i.e., a low-temperature deposition followed by a short-time annealing at intermediate temperature) in obtaining highly oriented PZT films on MgO-buffered oxidized silicon substrates. First, an oxide layer (10 nm thick) was thermally grown on a p -type (100)-Si wafer in dry oxygen. Then, a MgO film (10–50 nm thick) was sputter deposited on the oxidized Si. A PZT film (0.1–2.0 μm thick) was then sputter deposited on MgO-buffered substrates using the following conditions: rf power of 60 W, target–substrate distance of 1.5 in., argon/oxygen ambient of 15 mTorr, and substrate temperature of 100 °C. The PZT films were annealed at 600–650 °C for 10–20 min in air ambient using a conventional furnace.

The structural properties of the grown films were characterized by x-ray diffraction (XRD) analysis using $\text{Cu } K\alpha$ radiation. The interface properties of the MFIS structure were also characterized by measuring the elemental distributions on the cleaved cross sections of the specimens that were prepared with or without a MgO buffer layer. The elemental traces were obtained by energy-dispersive x-ray spectroscopy (EDS). The cross sections were scanned by an electron beam at 7 kV in a Philips XL30 scanning electron microscope with a field emission source and an EDAX ultrathin window detector. The intensities of the oxygen, silicon, and magnesium K , the zirconium $L\alpha$ and the lead $M\alpha$ lines were measured as a function of distance. From these results, the role of a MgO buffer as a diffusion barrier between PZT and oxidized Si has been investigated.

The dielectric constants of the insulating buffer and ferroelectric layers were characterized using a capacitance-versus-voltage (C - V) method. First, a MOS capacitor structure (i.e., the metal/ SiO_2 /Si structure) was fabricated, and the SiO_2 capacitance was read from the C - V curve measured in the accumulation region. Then, a metal/MgO/ SiO_2 /Si capacitor structure was formed on the same SiO_2 -buffered substrate, and C - V measurement was carried out on the stacked capacitor structure. Comparing the stacked capacitance value and the SiO_2 capacitance, the MgO capacitance was extracted. The dielectric constant of MgO was then calculated from this capacitance and the known value of the MgO thickness. Finally, a metal/PZT/MgO/ SiO_2 /Si capacitor structure was formed on the same MgO/ SiO_2 -buffered substrate, and C - V measurement was carried out. The stacked capacitance of PZT/MgO/ SiO_2 was extracted from the accumulation region capacitance value. The PZT capacitance was then extracted by comparing the stacked capacitance with the MgO/ SiO_2 capacitance measured before. The capacitance of the PZT layers of the MFIS structure studied in this work is found to be constant (i.e., independent of the gate voltage) in the accumulation region of the C - V curve. The effective linear dielectric constant of PZT was then defined, and its value was extracted from the measured capacitance and known thickness values of the PZT layer. The memory window of the PZT/MgO/ SiO_2 /Si structure was also characterized with a C - V method. The C - V measurement was performed at 1 MHz with a small signal voltage of 15 mV. The dc bias was swept at a 1 V/min rate. For C - V measurement, electrodes were prepared on both the top and bottom faces of the specimens. First, the backside of the wafer was etched in BHF solution in order to remove any oxide. During the etching process, the front surface was protected with a photoresist. An aluminum film was then deposited on the back surface by thermal evaporation. Postdeposition annealing was performed at 500 °C for 20 min in order to obtain ohmic contact. Aluminum top electrodes were prepared on the top film surface by thermal evaporation. A 0.5- or 0.7-mm-diam shadow mask was used to define the electrode area.

IV. RESULTS AND DISCUSSIONS

A. Structural properties

Figure 4(a) shows XRD $\theta/2\theta$ scan profiles of the samples that have a 1.0- μm -thick PZT film deposited on MgO-buffered (MgO thickness of 20, 30, and 50 nm), oxidized (SiO_2 thickness of 10 nm) Si. The XRD pattern of a sample grown without a MgO buffer is also shown for comparison. The PZT films grown on MgO-buffered substrates clearly show perovskite phase formation, whereas the PZT grown without a MgO buffer is amorphous or poorly crystallized. [The XRD of the PZT grown without a MgO buffer shows a small peak at the (110)-PZT position at 31°. However, the peak intensity is much weaker than those of the PZT with a MgO buffer.] This dramatic difference demonstrates the usefulness of a MgO buffer in obtaining highly crystallized PZT films on an amorphous surface. The orientation of PZT films varies depending on the MgO thickness, i.e., the PZT is mostly (111) oriented on 20 nm MgO, (100)

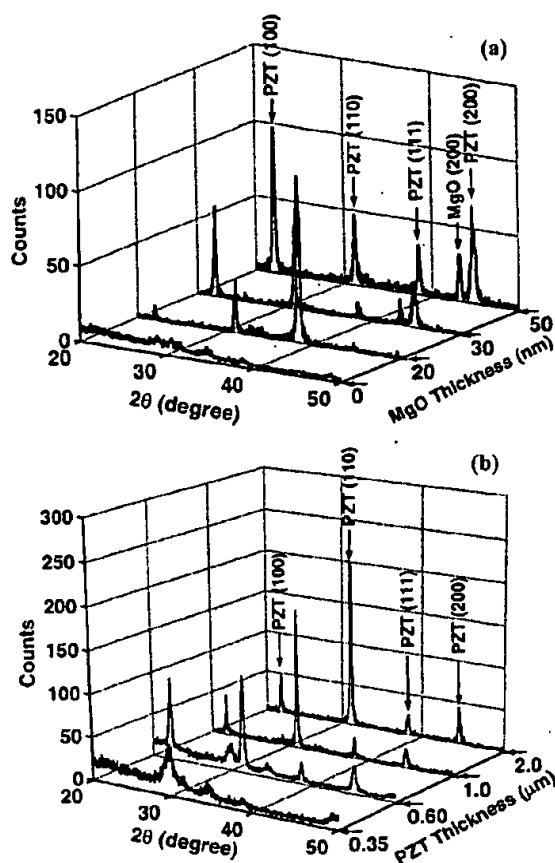


FIG. 4. (a) XRD $\theta/2\theta$ scan profiles of 1.0- μm -thick PZT films deposited on MgO-buffered (MgO thickness of 20, 30, and 50 nm), oxidized (SiO_2 thickness of 10 nm) Si substrates. The PZT film grown without a MgO buffer is also shown for comparison. (b) XRD $\theta/2\theta$ scan profiles of PZT films (PZT thicknesses of 0.35, 0.6, 1.0, and 2.0 μm) grown on MgO-buffered (MgO thickness of 10 nm), oxidized (SiO_2 thickness of 10 nm) Si substrates.

and (110) oriented on 30 nm MgO, and mostly (100) oriented on 50 nm MgO. It is interesting to note that the PZT films grown on the MgO buffered substrates show similar intensities of the PZT peaks despite their orientation difference among the samples. This suggests that the degree of crystallization in PZT films might be nearly the same among the samples grown with different MgO thickness in the range of 20 nm or greater.

It should also be noted in Fig. 4(a) that the XRD analysis clearly reveals a peak at the MgO(200)-plane position for MgO thickness of 30 or 50 nm. This shows that MgO has a strong tendency to grow highly oriented even on an amorphous substrate. The MgO peak becomes weaker and finally disappears as the film thickness is reduced to 20 nm or below. It is unclear at this stage whether significant crystallization has occurred in the 20-nm-thick MgO film or not, since the film thickness might be too thin to produce any measurable intensity of x-ray diffraction. Considering the near-constant degree of PZT crystallization on 20–50-nm-thick MgO buffers, however, we can speculate that even 20-nm-thick MgO might be grown with some orientation. This

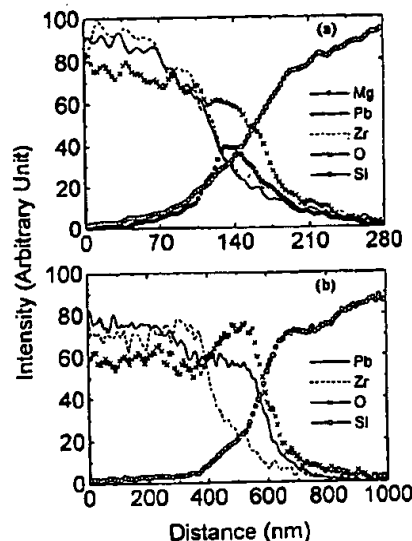


FIG. 5. EDS profiles of O, Si, Pb, Zr, and Mg measured on the cross section of the PZT/MgO(40 nm)/ SiO_2 (10 nm)/Si structure (a), and of the PZT/ SiO_2 (10 nm)/Si structure (b). In both cases, the PZT films were deposited at 100 $^{\circ}\text{C}$ and then annealed at 600 $^{\circ}\text{C}$ for 20 min in air ambient. Please note the different scales for distance.

speculation is further supported by a report that the MgO molecules tend to form well-aligned, small three-dimensional crystallites right at the inception of the deposition, i.e., at the nucleation stage, with the (100) planes as a preferred out-of-plane alignment.¹³ The dependence of the PZT orientation on MgO thickness [as observed in Fig. 3(a)] then suggests that the dominance of the (100) planes may not have fully established yet in MgO for thickness of 20 nm or less.

Figure 4(b) shows XRD profiles of the samples that have a PZT film grown on 10-nm-thick MgO-buffered, oxidized (SiO_2 thickness of 10 nm) Si. The PZT thickness was varied in a broad range (0.35, 0.6, 1.0, and 2.0 μm). At the PZT thickness of 1 or 2 μm , the (110)-PZT peak at 30.4 $^{\circ}$ is found predominant over others such as the (100) and (111) peaks. At the PZT thickness of 0.6 μm , a new peak appears at 29.8 $^{\circ}$, and it becomes a dominant one at 0.35 μm thickness of PZT. Considering that the composition of our sputter target is near the morphological phase boundary, the peak at 29.8 $^{\circ}$ is ascribed to the (101) peak of the tetragonal phase PZT.¹⁴ The MgO buffer (i.e., the orientation of the 10-nm-thick MgO buffer) seems to play an important role in determining/influencing the PZT orientation [i.e., the shift of the dominant peak from the (101) to the (110) orientation for PZT thickness greater than 0.3 μm]. The mechanism of this orientation change is not fully understood and is the subject of further study.

B. Interface properties

Figure 5(a) shows the EDS analysis result on the elemental traces for the specimens that have a 1.0- μm -thick PZT film deposited on 40-nm-thick MgO-buffered, oxidized (SiO_2 thickness of 10 nm) Si. The result without a MgO

buffer is also shown in Fig. 5(b) for comparison. All specimens experienced a postdeposition anneal treatment at 600 °C for 20 min in air ambient. In Fig. 5(a), a MgO buffer layer is clearly shown in between the PZT layer and the SiO₂/Si substrate. Both the lead and zirconium profiles are well confined on the PZT film side without any noticeable diffusion through the MgO buffer layer. In contrast, Fig. 5(b) shows a clear shift of the lead distribution toward the substrate side (as evident from comparison of the lead and zirconium traces), and also the corresponding increase in O counts. This indicates that a lead silicate layer is formed at the interface by oxidation of silicon and reaction with the PZT. Overall, the result demonstrates a 40-nm-thick MgO buffer serves well as a barrier between the PZT and an oxidized Si substrate.

C. *C-V* measurement and dielectric constants

C-V analyses were carried out on the metal/SiO₂/Si, metal/MgO/SiO₂/Si, and metal/PZT/MgO/SiO₂/Si structures (with 0.5-mm-diam Al electrodes). Figure 6(a) shows the *C-V* characteristics of the metal/SiO₂/Si structure that has a thermally grown SiO₂ of 12 nm thickness. The *C-V* curve clearly shows the regions of accumulation, depletion, and inversion. The accumulation region capacitance is read to be 500 pF. Assuming the SiO₂ dielectric constant of 3.9ε₀, the oxide thickness is calculated to be 13 nm, which is in reasonably good agreement with the value expected based on our calibration (oxide thickness versus oxidation time). Figure 6(b) shows the *C-V* measurement result of a metal/MgO(12 nm)/SiO₂(12 nm)/Si sample. The capacitance value in the accumulation region is read to be 360 pF. Comparing with the capacitance of the metal/SiO₂/Si sample, the MgO capacitance is calculated to be 1.3 nF. From the known thickness value of MgO, the dielectric constant of the MgO layer is then calculated to be 8.9ε₀, which is in good agreement with the bulk material's data. Figure 6(c) shows the *C-V* curve of a metal/PZT(350 nm)/MgO(12 nm)/SiO₂(12 nm)/Si sample. The accumulation region capacitance is read to be 185 pF. Comparing this capacitance value with that of the metal/MgO/SiO₂/Si structure, the capacitance of the 350-nm-thick PZT layer is estimated to be 380 pF. It should also be noted that the accumulation region capacitance of the MFIS structure remains nearly constant in this voltage sweep of -5 to 0 V. This indicates that the *P-E* hysteresis is far below the saturation regime in this voltage range. The ferroelectric polarization (*P_d*) is then expected to show a near-linear relationship to the electric field (*E*), as was discussed in Fig. 2(a).

The PZT capacitance *C_{PZT}* extracted in the way described above comprises contributions from both the linear dielectric component and the switchable ferroelectric polarizations, and can be expressed as follows:

$$C_{PZT} = \frac{dQ}{dV} = \frac{A}{t_f} \frac{d(\epsilon_f E_f + P_d)}{dE_f} = \frac{A}{t_f} \left(\epsilon_f + \frac{dP_d}{dE_f} \right), \quad (14)$$

where *A* is the area of the capacitor electrode and *t_f* is the thickness of the PZT layer. The slope of the *P_d* vs *E_f* curves shows a nearly constant value in the nonsaturated regime. By

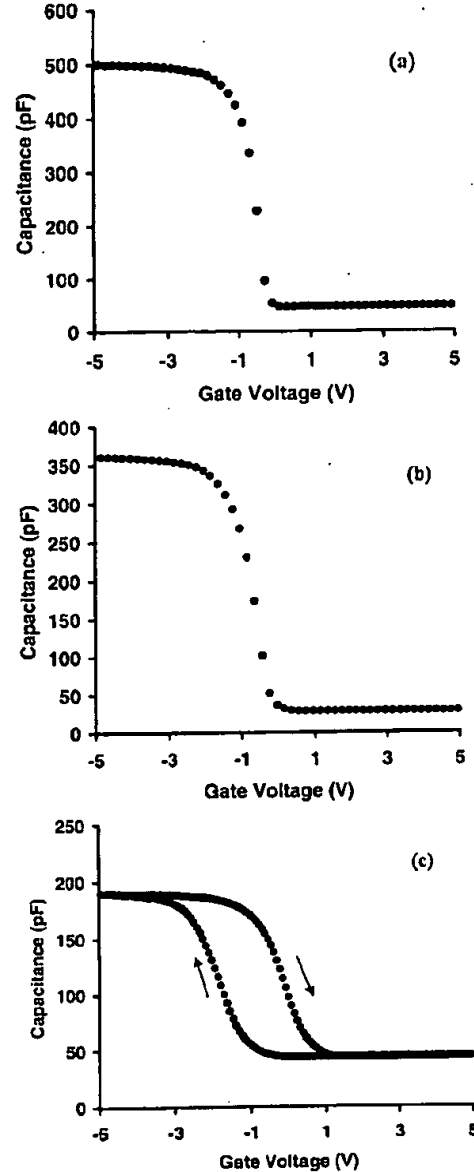


FIG. 6. Capacitance vs voltage (*C-V*) measurement results: (a) metal/SiO₂(12 nm)/Si sample, (b) metal/MgO(12 nm)/SiO₂(12 nm)/Si sample, and (c) metal/PZT(0.35 μm)/MgO(12 nm)/SiO₂(12 nm)/Si sample. The capacitor electrode area is 1.96 × 10⁻³ cm².

applying a first-order approximation on the *P-E* relationship described in Eqs. (9) and (12), and also assuming *P_r*/*P_s* ≈ 0.5, the slope can be expressed as follows:

$$\frac{dP_d}{dE_f} \approx \frac{P_s}{2E_c}, \quad (15)$$

Combining Eqs. (14) and (15), we can define an effective linear dielectric constant of PZT in the low-field regime as follows:

$$\epsilon_{eff} = \epsilon_f + \frac{P_s}{2E_c}. \quad (16)$$

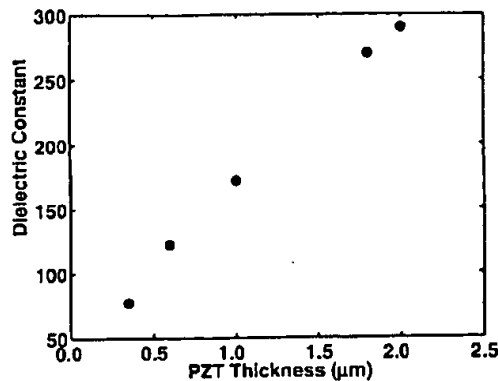


FIG. 7. Effective (linear) dielectric constants of PZT films that were estimated from the C - V measurement results for various different film thicknesses in the range of 0.35–2.0 μm .

From the measured capacitance value (380 pF) and the known thickness (350 nm) of the PZT layer, the effective linear dielectric constant ϵ_{eff} is estimated to be $77\epsilon_0$. It is important to mention that in this calculation the 0.35- μm -thick PZT layer is assumed to have a uniform distribution of the dielectric and ferroelectric constants throughout the film thickness.

The thickness of the PZT layer in the MFIS structure was varied in the range of 0.35–2.0 μm , and the effective linear dielectric constant ϵ_{eff} of the PZT layers was extracted from the C - V measurement result using the procedure described above. Figure 7 shows a summary of the measurement result for various different PZT thicknesses. The measured effective dielectric constant shows initially a low value of $70\epsilon_0$ at 0.35 μm thickness of PZT, and then monotonically increases to $280\epsilon_0$ at 2 μm thickness. According to Eq. (16), the effective linear dielectric constant of a single homogeneous layer (of constant dielectric/ferroelectric properties along the thickness direction) is expected to be independent of film thickness in the low-field regime. The observed strong dependence of the PZT dielectric constant on film thickness (Fig. 7) suggests some degree of inhomogeneity/nonuniformity of the PZT films along the thickness direction. In thin films studies, it is well known that film growth usually involves two distinct stages, i.e., an initial growth stage (of nucleation and coalescence) and a main growth stage of film bulk thickness. The crystallization in the initial nucleation layers is, in general, poor (and/or the crystallites are more randomly oriented than those in the main layers), and this structural difference usually results in different film properties in the electrical and other physical aspects. The nature of the initial layers (thickness and properties) depends on the details of the process conditions and the materials system.

D. Two-layer model of PZT films

In this study we have analyzed the thickness dependence of the measured PZT dielectric constants using a model that is based on the assumption that each PZT layer consists of two sublayers: a bottom layer of fixed thickness t_{f1} with the

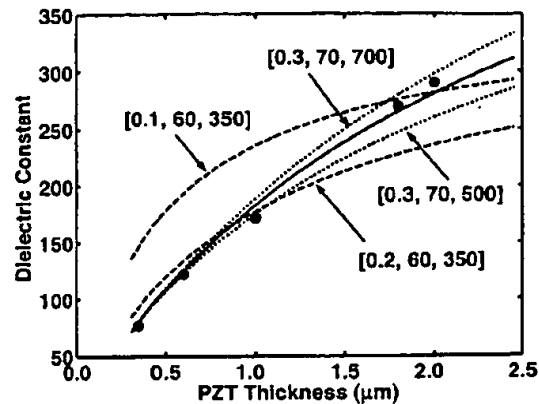


FIG. 8. Model predictions of the thickness dependence of the effective dielectric constant of PZT. The dashed curves correspond to the case that the bottom sublayer thickness t_{f1} is varied from 0.1 to 0.2 μm while the effective dielectric constants of the bottom and top sublayers are kept constant at $\epsilon_{\text{eff}1} = 60\epsilon_0$ and $\epsilon_{\text{eff}2} = 350\epsilon_0$. The dotted curves correspond to the case of $\epsilon_{\text{eff}2} = 500\epsilon_0$ or $700\epsilon_0$ with fixed values of $t_{f1} = 0.3 \mu\text{m}$ and $\epsilon_{\text{eff}1} = 70\epsilon_0$. The measurement result is also shown (the filled circles).

effective dielectric constant $\epsilon_{\text{eff}1}$ and a top layer of variable thickness t_{f2} with the effective dielectric constant $\epsilon_{\text{eff}2}$.^{15,16} The measured effective dielectric constant of a PZT layer would then correspond to a two-layer stacked capacitor structure, and can be expressed as follows using the model parameters assumed of each layer:

$$\epsilon_{\text{eff}} = \left[\frac{1}{\epsilon_{\text{eff}1}} + \frac{t_{f1}}{t_f} \left(\frac{1}{\epsilon_{\text{eff}1}} - \frac{1}{\epsilon_{\text{eff}2}} \right) \right]^{-1}, \quad (17)$$

where t_f is the total thickness of a PZT film, i.e., $t_f = t_{f1} + t_{f2}$. The model parameters (t_{f1} , $\epsilon_{\text{eff}1}$, and $\epsilon_{\text{eff}2}$) of our PZT films studied in this work were extracted by fitting the simulation result to the measurement data. In Fig. 8, for example, the dashed curves correspond to the case that the bottom sublayer thickness t_{f1} was varied from 0.1 to 0.2 μm while the effective dielectric constants of the bottom and top sublayers were kept constant at $\epsilon_{\text{eff}1} = 60\epsilon_0$ and $\epsilon_{\text{eff}2} = 350\epsilon_0$. The dotted curves correspond to the case of $\epsilon_{\text{eff}2} = 500\epsilon_0$ or $700\epsilon_0$ with fixed values of $t_{f1} = 0.3 \mu\text{m}$ and $\epsilon_{\text{eff}1} = 70\epsilon_0$. Similarly, the bottom sublayer's effective dielectric constant was also varied in a broad range while keeping the other two parameters at fixed values, although the result is not shown in Fig. 8. Overall, the best fit between the experimental and simulation results was obtained with $t_{f1} = 0.3 \mu\text{m}$, $\epsilon_{\text{eff}1} = 70\epsilon_0$, and $\epsilon_{\text{eff}2} = 700\epsilon_0$ as shown in Fig. 8 (the middle solid curve). It is interesting to relate this result to the XRD analysis result shown in Fig. 4(b). The 0.35- μm -thick PZT layer grown on MgO(100 nm)/SiO₂(100 nm)-buffered Si shows a relatively weak PZT peak at the (110)-orientation position. For PZT films thicker than 0.35 μm (i.e., 0.6, 1.0, and 2.0 μm), the dominant peak shifts to the (101) orientation with much stronger x-ray intensity. The x-ray profile remains nearly the same for thickness greater than 0.35 μm . The distinctive change of XRD patterns for film thickness of around 0.35 μm and above seems to support the two-layer model and the estimated model parameter values described

above, i.e., the bottom sublayer thickness t_{f1} of 0.3 μm , and the relatively low value of the effective dielectric constant of the bottom sublayer compared with that of the top sublayer (i.e., $\epsilon_{\text{eff}} = 70\epsilon_0$ vs $\epsilon_{\text{eff}} = 600\epsilon_0$). It should, however, be mentioned that the nature of the film properties, in general, depends on the process details (such as substrate, film deposition method, and conditions used), and would be variable to some extent.

E. Memory window

One of the primary goals of this study is to characterize the dielectric/ferroelectric properties of our films and to optimize the layer structure of the MFIS capacitors such that the devices show a maximum memory window with low-operating-voltage requirement. Both the experimental and simulation work were carried out in order to investigate the dependence of the memory window on the key structural parameter (i.e., the PZT layer thickness) and also the operating condition (the peak gate voltage applied). In the experimental work, a set of the MFIS capacitor structures were fabricated with the PZT thickness in the range of 0.1–2.1 μm while keeping the MgO and SiO₂ thickness constant at 10 nm each. The C - V measurements were then carried out on the MFIS capacitor structures, and a memory window was read from the C - V hysteresis curves. In the simulation work, the PZT films are assumed to have a two-layer structure when the film thickness is greater than 0.3 μm , and the dielectric/ferroelectric behavior of PZT in the MFIS structure was analyzed using the two-layer model described above.

1. Dependence of the memory window on the peak gate voltage

It is important to note that the amount of ferroelectric polarization switching depends on the peak gate voltage applied (of both positive and negative polarities). Figure 9 shows the C - V curves of the PZT(2.0 μm)/MgO(10 nm)/SiO₂(10 nm)/Si sample (with 0.7-mm-diam Al electrodes) measured with different voltage sweeps. First, the gate voltage was swept from +6 to -6 V (the solid curve). Then, a sweep was made from -6 to +6 V (the solid curve), and finally from +10 to -6 V (the dotted curve). Comparing the two sweeps that go to the negative direction, it is clear that the threshold voltage shifts towards the negative direction as the positive peak voltage (i.e., the starting voltage of the negative-going sweep) is increased from +6 to +10 V. Figure 9 shows the C - V curves of the same device, but with different sweep voltages. First, the gate voltage was swept from -6 to +6 V (the solid curve). Then, a sweep was made from +6 to -6 V (the solid curve), and finally, from -10 to +6 V (the dotted curve). Again, comparing the two positive-going sweeps, we observe a positive shift of threshold voltage as the negative starting voltage is increased in its magnitude.

The memory window is defined as a difference of the threshold voltage in the positive- and negative-going sweeps. It usually shows a monotonic increase as a function of peak gate voltage, and would eventually saturate when the P - E characteristic reaches the saturation regime. We have carried out numerical analysis on the dependence of the memory

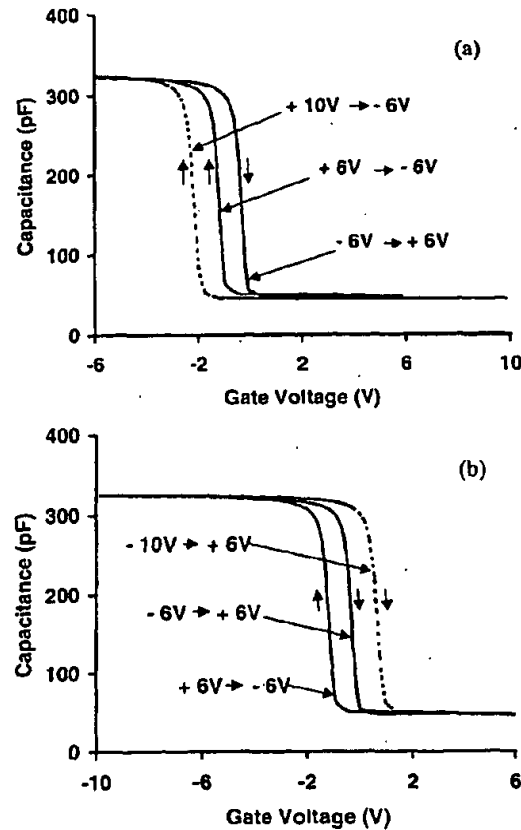


FIG. 9. C - V curves of a metal/PZT(2.0 μm)/MgO(10 nm)/SiO₂(10 nm)/Si structure measured with different voltage sweeps: (a) +6 to -6 V (solid), -6 to +6 V (dashed), and +10 to -6 V (dotted), (b) -6 to +6 V (solid), +6 to -6 V (dashed), and -10 to +6 V (dotted).

window on peak gate voltage, assuming proper dielectric/ferroelectric model parameters (i.e., ϵ_f , P_s , P_r , and E_c) for each sublayer of PZT films. The parameter values were then extracted by fitting the simulation result to the measurement data. In this numerical analysis, the boundary conditions and the formula for the gate voltage were properly modified (Eqs. (1) and (2)), taking into account the two-layer structure of PZT. The threshold voltage shift is then expressed as follows:

$$\Delta V_{\text{th}} = - \left(\frac{\Delta P_{d1}(E_{f1})}{C_{f1}} + \frac{\Delta P_{d2}(E_{f2})}{C_{f2}} \right). \quad (18)$$

where ΔP_{d1} and ΔP_{d2} are the amount of ferroelectric polarization switching in the bottom sublayer and in the top sublayer of PZT, respectively. E_{f1} and E_{f2} are the electric field in the respective layer of PZT. C_{f1} and C_{f2} represent the capacitance component of each layers of PZT that excludes the contribution from the switchable polarizations, and are given by

$$C_{f1} = \frac{\epsilon_{f1}}{t_{f1}} \quad (19)$$

and

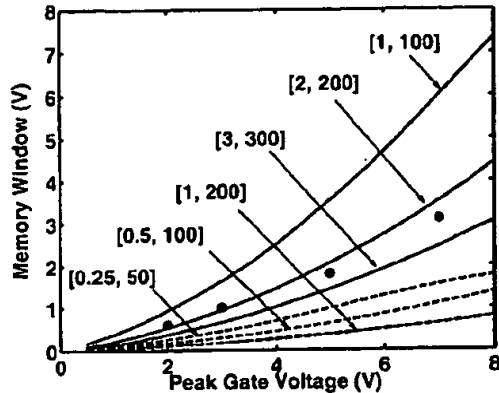


FIG. 10. Memory window vs peak gate voltage applied on a metal/PZT(0.35 μm)/MgO(10 nm)/SiO₂(10 nm)/Si structure. Filled circles correspond to the measurement data obtained with symmetric voltage sweeps of ± 2 , ± 3 , ± 5 , and ± 7 V. The solid curves correspond to the case of $\epsilon_{f1} = 10\epsilon_0$ with $[P_{s1}, E_{c1}] = [1 \mu\text{C}/\text{cm}^2, 100 \text{ kV}/\text{cm}]$, $[2 \mu\text{C}/\text{cm}^2, 200 \text{ kV}/\text{cm}]$, and $[3 \mu\text{C}/\text{cm}^2, 300 \text{ kV}/\text{cm}]$. Dashed curves correspond to the case of $\epsilon_{f1} = 40\epsilon_0$ with $[P_{s1}, E_{c1}] = [0.25 \mu\text{C}/\text{cm}^2, 50 \text{ kV}/\text{cm}]$, $[0.5 \mu\text{C}/\text{cm}^2, 100 \text{ kV}/\text{cm}]$, and $[1 \mu\text{C}/\text{cm}^2, 200 \text{ kV}/\text{cm}]$.

$$C_{f2} = \frac{\epsilon_{f2}}{t_{f2}}, \quad (20)$$

where ϵ_{f1} and ϵ_{f2} are the linear dielectric constants of the top and bottom sublayers of PZT, respectively, and t_{f1} and t_{f2} are the corresponding layer thicknesses. In this two-layer model, the P - E characteristic is described with the parameters P_{s1} , P_{r1} , and E_{c1} for the bottom layer, and with P_{s2} , P_{r2} , and E_{c2} for the top layer part of PZT. As was discussed in Sec. IV C, the effective dielectric constant ϵ_{eff} comprises both the linear dielectric constant component and the switchable ferroelectric polarization component, and can be expressed as $\epsilon_{\text{eff}} = \epsilon_f + P_s/2E_c$ according to Eq. (16). The ϵ_{eff} value is estimated to be $70\epsilon_0$ and $600\epsilon_0$ for the bottom and top layer parts, respectively. In this work, two MFIS capacitor samples with PZT thickness t_f of 0.35 or 0.60 μm were chosen for measurement of the memory window versus peak gate voltage and also for extraction of the model parameters. In the case of the sample with $t_f = 0.35 \mu\text{m}$, the top sublayer part of PZT is estimated to be only 0.05 μm , much thinner than the 0.3- μm -thick bottom sublayer part. Considering, also, the relatively large value of the measured effective dielectric constant of the top layer, the top layer part is expected to have a negligible effect on the observed memory window. The presence of the 0.05- μm -thick top layer part was, therefore, neglected for simplicity of numerical work, and the model parameters of the bottom layer were extracted from these data. The top layer's model parameters were then extracted from the measurement result of the sample with $t_f = 0.6 \mu\text{m}$ in conjunction with the bottom layer parameters extracted from the sample with $t_f = 0.35 \mu\text{m}$.

Figure 10 (the filled circles) shows the memory window of a PZT(0.35 μm)/MgO(10 nm)/SiO₂(10 nm)/Si sample measured as a function of the peak gate voltage applied with a symmetric voltage sweep. The memory window is measured to be 0.6 V for ± 2 V sweep, 1.0 V for ± 3 V, 1.8 V for

± 5 V, and 3.1 V for ± 7 V. The monotonic increase of the memory window indicates that the PZT films are in the unsaturated regime in this voltage range. The solid and dashed curves in Fig. 10 correspond to the simulation result with various different parameter values of ϵ_{f1} , P_{s1} , and E_{c1} . The parameter values were varied in a broad range while satisfying the constraint, $\epsilon_{f1} + P_{s1}/2E_{c1} = 70\epsilon_0$. The solid curves correspond to the case of $\epsilon_{f1} = 10\epsilon_0$ with $[P_{s1}, E_{c1}] = [1 \mu\text{C}/\text{cm}^2, 100 \text{ kV}/\text{cm}]$, $[2 \mu\text{C}/\text{cm}^2, 200 \text{ kV}/\text{cm}]$, and $[3 \mu\text{C}/\text{cm}^2, 300 \text{ kV}/\text{cm}]$. The dashed curves correspond to the case of $\epsilon_{f1} = 40\epsilon_0$ with $[P_{s1}, E_{c1}] = [0.25 \mu\text{C}/\text{cm}^2, 50 \text{ kV}/\text{cm}]$, $[0.5 \mu\text{C}/\text{cm}^2, 100 \text{ kV}/\text{cm}]$, and $[1 \mu\text{C}/\text{cm}^2, 200 \text{ kV}/\text{cm}]$. In this simulation, the ratio P_r/P_s was assumed to be 0.4 for the bottom sublayer. The parameter values that give the best fit are found to be $\epsilon_{f1} = 10\epsilon_0$, $P_{s1} = 3.0 \mu\text{C}/\text{cm}^2$, and $E_{c1} = 280 \text{ kV}/\text{cm}$. Following a similar procedure with the measurement result of a PZT(0.60 μm)/MgO(10 nm)/SiO₂(10 nm)/Si sample (the measurement data are not shown in this article), the top layer's model parameters were also extracted as follows: $\epsilon_{f2} = 200\epsilon_0$, $P_{s2} = 8 \mu\text{C}/\text{cm}^2$, and $E_{c2} = 100 \text{ kV}/\text{cm}$. Ratio P_r/P_s of the top sublayer was assumed to be 0.5 in this simulation. It should be noted that the saturated polarization of the top layer (P_{s2}) is larger than that of the bottom layer (P_{s1}), while the coercive field of the top layer (E_{c2}) is smaller than that of the bottom layer (E_{c1}). This result is consistent with the XRD analysis discussed before, which suggests that the top layer part of PZT is more highly oriented than the bottom layer part. It is also interesting to note that the linear dielectric constant of the top layer is much larger than the bottom layer's ($\epsilon_{f2} = 200\epsilon_0$ vs $\epsilon_{f1} = 10\epsilon_0$), although the physical reason is not clearly understood at this stage. Using these parameter values, we have also calculated the polarization switching in each sublayer of PZT. Figures 11(a) and 11(b) show the polarization versus gate voltage (P - V) curves in the bottom sublayer (0.30 μm thick) and top sublayer (0.05 μm thick) of a PZT(0.35 μm)/MgO(10 nm)/SiO₂(10 nm)/Si sample, respectively. The amount of polarization switching with ± 7 V sweep is read to be $0.1 \mu\text{C}/\text{cm}^2$ for the bottom layer and $0.05 \mu\text{C}/\text{cm}^2$ for the top layer. Using Eqs. (18)–(20), the total amount of the threshold voltage shift is calculated to be 3.40 V with a contribution of 3.39 V from the bottom layer and 0.01 V from the top layer. This result validates the approximation used in extracting the bottom layer parameters from the 0.35 μm sample, i.e., neglecting the presence of the 0.05- μm -thick top layer.

2. Dependence of the memory window on the PZT thickness

Using the PZT model parameter values extracted above, i.e., P_{s1} , P_{r1} , E_{c1} , ϵ_{f1} , and t_{f1} for the bottom layer and P_{s2} , P_{r2} , E_{c2} , and ϵ_{f2} for the top layer part of PZT, we have calculated the dependence of the memory window on the PZT layer's thickness in the metal/PZT/MgO/SiO₂/Si structure. The PZT thicknesses were varied from 0 to 2.5 μm while the MgO and SiO₂ thickness was kept constant at 10 nm each. The gate voltage was swept for ± 5 V in this simulation. Figure 12 shows the simulation result (the solid curve) and also a measurement result obtained from the

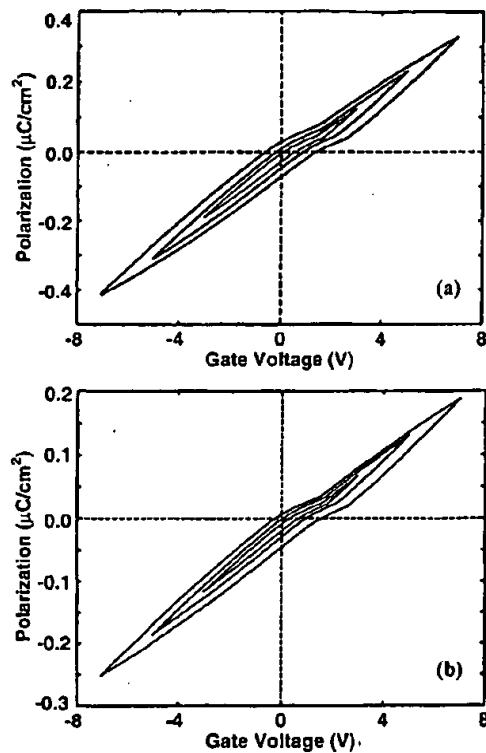


FIG. 11. Simulation results of polarization vs peak gate voltage applied on the MFIS structure described in Fig. 10. (a) P - V for the 0.30- μm -thick bottom sublayer part of PZT. (b) P - V curve for the 0.05- μm -thick top sublayer part of PZT.

samples with PZT thicknesses of 0.1, 0.35, 0.6, 1.0, 1.8, and 2.0 μm (the filled circles). The memory window shows a peak value of 1.8 V at the PZT thickness of 0.3 μm . Experimentally, we have obtained 1.78 V of the memory window at 0.35 μm thickness. Overall, the simulation curve shows a good fit to the experimental data. This supports the validity of using the two-layer model and their extracted parameter values for the PZT-based MFIS structures studied in this work. We have also calculated the thickness dependence of the memory window assuming a single-layer model of PZT. The dotted curve shows a simulation result with parameter values of $P_s = 3 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.4$, $E_c = 280 \text{ kV}/\text{cm}$, and $\epsilon_f = 10\epsilon_0$, the same as the bottom sublayer's of the two-layer model discussed above, and the dashed curve with $P_s = 8 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.5$, $E_c = 100 \text{ kV}/\text{cm}$, and $\epsilon_f = 200\epsilon_0$, the same as the top layer's. It is interesting to note that a single-layer model with the parameter values of the bottom layer produces a somewhat similar profile, although it predicts a larger memory window than the measurement result (and also the simulation with the two-layer model) for PZT thickness greater than around 0.35 μm . This overestimation is ascribed to that the PZT layer gets a stronger electric field due to the assumption of a much lower dielectric constant and, therefore, the estimated polarization switching is larger. Besides the validity of the two-layer model, this simulation also shows that the bottom sublayer, which has a

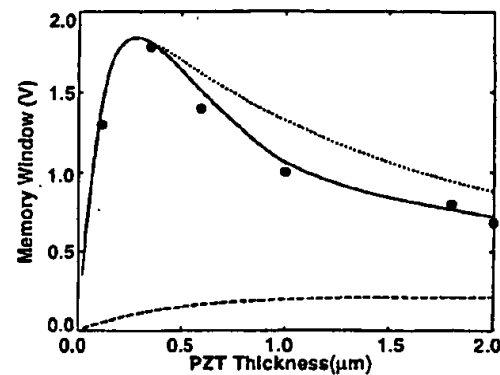


FIG. 12. Dependence of the memory window on PZT thickness in a metal/PZT/MgO(10 nm)/SiO₂/Si structure. Filled circles correspond to the measurement result with a $\pm 5 \text{ V}$ sweep. Solid curve shows the simulation result obtained assuming a two-layer model for PZT with $P_s = 3 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.4$, $E_c = 280 \text{ kV}/\text{cm}$, and $\epsilon_f = 10\epsilon_0$ for the bottom sublayer and $P_s = 8 \mu\text{C}/\text{cm}^2$, $P_r/P_s = 0.5$, $E_c = 100 \text{ kV}/\text{cm}$, and $\epsilon_f = 200\epsilon_0$ for the top sublayer. The dotted curve corresponds to the simulation result obtained assuming a single-layer model with the parameter values of the bottom layer, and the dashed curve represents the simulation with a single-layer model with the parameter values of the top sublayer.

much lower effective dielectric constant, plays a more important role in determining the memory window.

The thickness dependence of the memory window in the MFIS structure can be understood in terms of the behavior of the two factors involved, i.e., ΔP_d and C_f in the memory window expression described in Eq. (8). According to our numerical analysis, each factor is found to show different thickness dependences, i.e., $\Delta P_d \propto (1 + t_f^\alpha)^{-1}$ with $\alpha = 1.47$ and $C_f \propto t_f^{-1}$. In the thin layer regime (less than 0.3 μm), the overall behavior is mostly governed by the thickness dependence of capacitance C_f . Therefore, the memory window sharply (nearly linearly) increases as a function of the PZT thickness. In the thick layer regime (greater than 0.3 μm), the decreasing tendency of ΔP_d overcompensates the increasing trend of C_f^{-1} , and this results in the overall dependence of $t_f^{-0.47}$. From the device design point of view, it would be desirable to maximize the memory window for a given voltage sweep. In that sense, 0.3 μm of PZT thickness is considered optimum. It is important to mention that the optimum thickness depends on the dielectric/ferroelectric properties of PZT and the buffer layers, and therefore, can be tailored to a desirable range. For example, decreasing the linear dielectric constant of PZT would allow for a steeper increase of the memory window, and thus a reduction of the optimum thickness. Similarly, tuning the coercive field and saturated polarization would result in further reduction of the optimum PZT thickness as was discussed in Sec. II.

V. CONCLUSIONS

We have investigated the structural and electrical properties of the MFIS structure that incorporates a MgO/SiO₂ insulating buffer between a ferroelectric layer and Si substrate. Highly oriented lead PZT films were grown on the MgO-buffered oxidized silicon substrates with a rf magnetron sputtering technique. The XRD and EDS analysis results

show that a MgO buffer serves well not only as a template layer for growing oriented PZT films on an amorphous surface but also as a diffusion barrier between PZT and Si substrates. The memory window of the MFIS structure was characterized with a $C-V$ method. Numerical analyses were also carried out to simulate the MFIS capacitor characteristics. In this simulation, the PZT films were assumed to have a two-layer structure in which the dielectric and ferroelectric properties of an initial layer are significantly weaker than those of the main layer part. By comparing the measurement data with the simulation result, we have extracted the parameters of this two-layer model (dielectric constant and the polarization versus electric-field characteristics) of the PZT films in the MFIS structure. The scalability of the memory window of the MFIS structure was investigated by varying the ferroelectric (PZT) layer thickness. Both the experimental and simulation results show that the PZT-based MFIS structure is suitable for nonvolatile memory field-effect transistors with low-voltage requirement (3 V or less) and a large memory window (1–2 V).

ACKNOWLEDGMENTS

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Declaration

Growth of highly oriented $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$ films on MgO-buffer d oxidized Si substrat s and its application to f rroel ctric nonvolatil m mory fi ld- ff ct transistors

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We have grown highly oriented lead zirconate titanate [$\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$ or PZT] films on oxidized silicon substrates using a thin MgO buffer layer (7–70 nm thick). Ferroelectric nonvolatile memory field-effect transistors (FETs) were successfully fabricated using the metal/PZT/MgO/SiO₂/Si structure in conjunction with radio-frequency sputter deposition of PZT and MgO films. The fabricated devices show excellent performance in ferroelectric polarization switching and memory retention. The results indicate that a thin MgO buffer serves well not only as a template layer for the growth of oriented PZT films on amorphous substrates, but also as a diffusion barrier between a ferroelectric and a substrate during device fabrication, protecting the SiO₂/Si interface and the FET channel region. © 1998 American Institute of Physics. [S0003-6951(98)03652-3]

A ferroelectric field-effect transistor (FEFET) consists of a FET whose gate dielectric is comprised of a ferroelectric material or a stack of dielectrics with a ferroelectric layer.¹ The application of a voltage pulse to the gate sets the direction of the ferroelectric polarization. The polarization direction controls the electrical conductance of the channel under the ferroelectric, and thus the drain current of the FET. The binary level of the channel conductance can be used to define two logic states, and can be read without destroying the ferroelectric polarization. Although the FEFETs offer unique advantages over other ferroelectric memories, to the best of our knowledge there has been no report of realization of commercially viable FEFETs. This is attributed to the various issues related to the structure, material, and/or fabrication processes that have been investigated so far. Among the various substrate materials appropriate for FEFETs, silicon is the most promising due to its commercial viability. The FEFETs on silicon have been investigated mainly with a metal/ferroelectric/semiconductor (MFS) gate structure using various different ferroelectric materials, such as $\text{Bi}_4\text{Ti}_3\text{O}_{12}$, BaMgF_4 , and LiNbO_3 .^{2–4} In the MFS-FETs, a ferroelectric makes a direct contact with silicon. This usually results in a high density of surface states caused by interdiffusion or reaction between the two materials or by the presence of a large number of unattended dangling bonds of Si atoms. A partial solution to this problem was reported that incorporates a proper buffer layer between the ferroelectric and silicon, such as CaF_2 , CeO_2 , or SrTiO_3 .^{5–7} These insulating buffer layers have a lattice structure similar to that of the ferroelectric and silicon, and therefore, help grow highly oriented ferroelectric films. These metal/ferroelectric/insulator/semiconductor (MFIS) structures showed improved interface properties compared with the MFS case. Nevertheless, the problems of retention, carrier injection, and large leakage

current still make it difficult to obtain commercially viable ferroelectric FETs. Recently, $\text{SrBi}_2\text{Ta}_2\text{O}_9/\text{CeO}_2/\text{SiO}_2/\text{Si}$ and $\text{SrBi}_2\text{Ta}_2\text{O}_9/\text{SiN}/\text{Si}$ structures were reported with good memory window in its capacitor characteristic.^{8,9} However, reports are not available on the performance of a nonvolatile memory FEFET device of those structures.

In this letter we report a FEFET that incorporates a thin, magnesium oxide (MgO) buffer layer between a ferroelectric $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$ (PZT) layer and an oxidized silicon substrate. The idea of using this two-layer-buffer structure (i.e., MgO/SiO₂) for a ferroelectric gate is based on the following reasons. First, it was found that PZT films can be grown highly oriented on MgO-buffered oxidized silicon substrates. Second, MgO has been widely used as a diffusion barrier for various materials systems, because of its refractory nature.¹⁰ The use of a MgO buffer, therefore, is expected to result in protecting the silicon FET channel region from interdiffusion or reaction with a ferroelectric layer during device processing. Third, thermal oxidation of Si has been known to be one of the best ways of passivating silicon surfaces. Therefore, the use of a (thermally grown) SiO₂ buffer in conjunction with a MgO buffer will allow us to produce (and keep) FET channels of good quality.

PZT is a well-known ferroelectric material. Recently, we have reported on crystallization of PZT films that were deposited on Pt-buffered oxidized silicon substrates using radio-frequency (rf) magnetron sputtering of a stoichiometric $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$ target (Zr:Ti ratio of 53:47).¹¹ PZT films deposited at 200 °C or below were found to crystallize into a perovskite phase upon receiving the anneal treatment at 590 °C or above. In this work, we have investigated the use of a MgO buffer layer in obtaining highly oriented PZT films on oxidized silicon substrates. First, an oxide layer (10–100 nm thick) was thermally grown on a *p*-type (100)-Si wafer in dry oxygen. Then, a 7–100-nm-thick MgO film was sputter deposited on the oxidized Si. A 0.3–2.7- μm -thick PZT film

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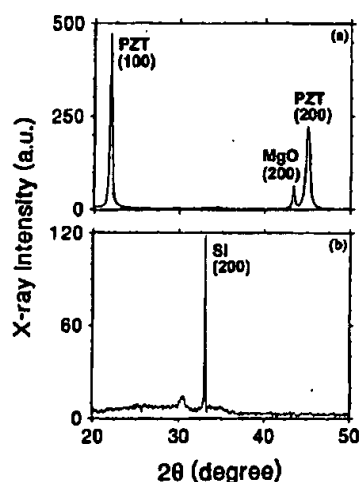


FIG. 1. X-ray diffraction $\theta/2\theta$ scan profiles of PZT films: (a) deposited on a MgO-buffered oxidized silicon substrate and (b) deposited on an oxidized silicon substrate. The thickness of the PZT, MgO, and SiO_2 films is 1 μm , 70 nm, and 50 nm, respectively.

was then sputter deposited on MgO-buffered substrates using the following conditions: rf power of 60 W, target-substrate distance of 1.5 in., argon/oxygen ambient of 15 mTorr, and substrate temperature of 100 °C. The PZT films were annealed at 600–650 °C for 10–20 min in air ambient using a conventional furnace.

Figure 1(a) shows an x-ray diffraction (XRD) $\theta/2\theta$ scan profile of a sample that has a 1.0- μm -thick PZT film deposited on a 70-nm-thick MgO-buffered, oxidized (SiO_2 thickness of 50 nm) Si. The profile shows that PZT is highly *c*-axis oriented, i.e., no other PZT peak is observed except for (100) and (200) for the scan range of 20°–70°. The (200)-MgO peak is also clearly observed, indicating that MgO tends to grow highly oriented even on an amorphous substrate. This result is consistent with a recent report by Wang *et al.* in which they were able to grow in-plane textured (100)-MgO films on amorphous Si_3N_4 substrates by ion-beam-assisted deposition.¹² (Regarding the texturing process, the paper reports that the MgO molecules form well-aligned, small three-dimensional crystallites right at the inception of the deposition, i.e., at the nucleation stage, with the (100) planes as a preferred out-of-plane alignment.) PZT films were also deposited on an oxidized Si without a MgO buffer and were compared with the films grown with MgO. For fair comparison, sputter deposition and anneal treatment of PZT films were carried out under the same conditions as before. A dramatic difference is observed between the two films. PZT films grown without MgO are found to be amorphous [Fig. 1(b)], whereas PZT films grown on a MgO-buffered oxidized Si substrate are highly (100) oriented. This clearly demonstrates the usefulness of a MgO buffer layer in obtaining highly oriented PZT films on amorphous substrates.

In order to test the usefulness of a MgO layer as a diffusion barrier between a PZT layer and an oxidized Si, elemental distributions were measured on the cleaved cross sections of the specimens that were prepared with or without a MgO buffer layer. The elemental traces were obtained by

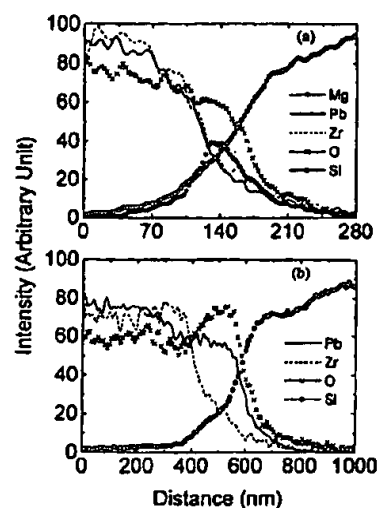


FIG. 2. EDS profiles of O, Si, Pb, Zr, and Mg measured on the cross section of the PZT/MgO(40 nm)/ SiO_2 (10 nm)/Si structure (a) and of the PZT/ SiO_2 (10 nm)/Si structure (b). In both cases, the PZT films were deposited at 100 °C and then annealed at 600 °C for 20 min in air ambient. Please note the different scales for distance.

energy dispersive x-ray spectroscopy (EDS). The cross sections were scanned by an electron beam at 7 kV in a Philips XL30 scanning electron microscope (SEM) with a field-emission source and an energy dispersive x-ray analysis ultrathin window detector. The intensities of the oxygen, silicon, and magnesium K, and the zirconium $L\alpha$ and the lead $M\alpha$ lines were measured as a function of distance. Figures 2(a) and 2(b) show the traces for the specimen that has a PZT film deposited on an oxidized (SiO_2 thickness of 10 nm) silicon substrate with or without a 40-nm-thick MgO buffer, respectively. Both specimens experienced a postdeposition anneal treatment at 600 °C for 20 min in air ambient. In Fig. 2(a), a MgO buffer layer is clearly shown in between the PZT layer and the SiO_2 /Si substrate. Both the lead and zirconium profiles are well confined on the PZT film side without any noticeable diffusion through the MgO buffer layer. In contrast, Fig. 2(b) shows a clear shift of the lead distribution toward the substrate side (as evident from comparison of the lead and zirconium traces), and also the corresponding increase in O counts. This indicates that a lead silicate layer is formed at the interface by oxidation of silicon and reaction with the PZT. The result demonstrates the usefulness of a MgO buffer as a barrier between the PZT and an oxidized Si substrate. The extensive results obtained in this work will be published in detail elsewhere.

We fabricated the FEFET devices using the metal/PZT/MgO/ SiO_2 /Si structure. The devices were fabricated on *p*-type (100)-Si wafers with the following dimensions: the channel width W of 100–500 μm and the channel length L of 20–160 μm with an aspect ratio W/L in the range of 3–5. Figure 3 shows the drain current I_D (i.e., the channel current) versus the drain-source voltage V_{DS} of a FEFET that has a 2.7- μm -thick PZT film grown on a 100-nm-thick MgO-buffered, oxidized (SiO_2 thickness of 100 nm) Si substrate. Prior to the I – V scans, +15 V or –15 V “write” voltage was applied to the gate for 1 s in order to enhance or to reduce the *n*-type channel conductance (i.e., to

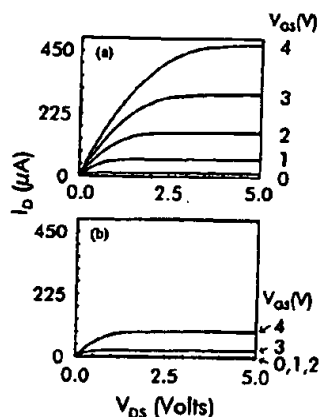


FIG. 3. The drain current (I_D) vs. drain-source voltage (V_{DS}) curves of a PZT/MgO/SiO₂/Si FEFET: (a) after a +15 V "write" pulse was applied to the gate and (b) after a -15 V "write" pulse was applied to the gate. The "read" gate voltages (V_{GS}) are 0, 1, 2, 3, and 4 V for both cases.

write "1" or "0"), respectively. Figure 3(a) shows the I - V curves measured after writing "1." The I_D - V_{DS} scans were carried out for the gate-source voltage V_{GS} (i.e., "read" voltage) of 0, 1, 2, 3, and 4 V. The result shows a I - V characteristic, typical of n -channel metal-oxide-semiconductor field-effect transistors (MOSFETs). The threshold voltage is estimated to be approximately 0 V, as read from Fig. 3(a). Figure 3(b) shows the I - V characteristic after writing "0." Comparing with the case of writing "1," a dramatic difference is observed. The channel current is significantly reduced and the threshold voltage increased to approximately 2 V. This result is consistent with the polarity of the writing voltage applied to the gate. In other words, the positive "write" voltage (+15 V) sets the ferroelectric polarization in the upward direction, which in turn induces (or enhances) an electron channel near the surface of the Si substrate. The negative "write" voltage (-15 V) reverses the ferroelectric polarization to the downward direction, thus depletes electrons in the channel region and, therefore, resulting in the increase of a threshold voltage. Overall, the result clearly demonstrates that the FET channel conductance can be switched between the low and high levels via the ferroelectric polarization reversal controlled by a gate voltage.

The threshold voltage change in a FEFET is due to the ferroelectric polarization switching, and the amount of the threshold voltage shift (the so-called memory window) is determined by various factors, such as materials and structural parameters and the amount of a "write" voltage applied.¹ Regarding the structural issue, reducing the buffer layer thicknesses would help decrease the operation voltage, since the voltage drop across each layer is inversely proportional to the capacitance of the layer. Regarding the materials issue, it would be desirable to tailor the ferroelectric properties of PZT films such that they show a significantly reduced

dielectric constant and maintains a large coercive voltage even at much reduced film thickness. In order to test the scalability of the structure in terms of both the operation voltage and the device dimension, we have reduced the buffer layer thicknesses to 10 nm and the PZT thickness to 0.3 μm . Although the result is not shown in this letter, the structure with this reduced dimension shows a significant decrease in voltage requirement, i.e., ± 7 V writing voltage for a 2 V memory window or ± 3 V writing voltage for a 1 V memory window.

The retention of memory of the fabricated FEFETs was tested over an extended period of time. The "1"-state channel current was found to reach a steady state after an initial, slight reduction (less than 5%) during the first one or two days. The "0"-state channel current does not show any noticeable change during this period. Retention tests over longer periods (over several weeks) were also carried out and no further degradation was detected. This demonstrates an excellent retention capability of the FEFET structure developed in this work, and is clearly contrasted to the poor retention of other previously reported FEFETs. Regarding the fatigue of the ferroelectric film, we reported excellent fatigue resistance of the PZT films that were deposited on Pt-coated oxidized silicon using the low-thermal-budget sputtering process: the films do not show any noticeable degradation even after 10^{12} cycles of polarization switching.¹¹ This suggests that the PZT films used in this work, i.e., the films deposited on MgO-buffered substrates using the same sputtering process, may also show excellent fatigue resistance. The fatigue test on the fabricated devices is being carried out and will be reported elsewhere. It is also interesting to note that the MgO's lattice structure (cubic) is similar to PZT's perovskite, which is a common structure of most ferroelectrics known in this area. This suggests the MgO/SiO₂ buffer layer structure should be applicable to other ferroelectrics as well.

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